Cont B1

/SSVTR. Until SSVTR and /SSVTR have changed their binary value, the enabled comparator in the receiver 405 detects whether change in signal binary value occurred.

The paragraph beginning at **page 12, line 4** has been amended to read as follows:

B2

FIG. 4 (4-1 and 4-2) is a high level schematic illustrating a single-ended signal slave 210, having a receiver 405 for each signal line 215. Each signal receiver 405 has two comparators 410, one comparator 410a for comparing an incoming single-ended signal "SNx" to SSVTR and the other comparator 410b for comparing SNx to /SSVTR. Both of the comparators 410 have output terminals selectively coupled via switches 415 to an output terminal 420. It will be appreciated that the output signal (SN) to the output terminal 420 is preferably a full rail signal (0V to 2.5V).

The paragraph beginning at **page 15, line 13** has been amended to read as follows:

B3

FIG. 5 (5-1 and 5-2) is a flowchart a method 500 of communicating signals from a master 205 across a transmission line 215 to a receiver 405. Method 500 begins with the master 205 in step 505 setting SSVTR to VOL and all single-ended signals (/SSVTR and SNx) to VOH, and in step 510 setting all single-ended receiver outputs (SN) to a full rail high. The receiver 405 in step 515 couples the comparator 410a, which compares SSVTR against each single-ended signal SNx, to the output terminal 420 of the receiver 405. The receiver 405 in step 517 lets all signals on the transmission lines settle down. Steps 505-517 are referred to as system initialization.

The paragraph beginning at **page 17, line 6** has been amended to read as follows:

B4

For a uniformly transitioning ramp-like signal, the preferred slew rate of signals is four times the sum of two inverter delays and an exclusive-OR delay in a given technology. In 0.25μ CMOS technology with an operating voltage of 2.5V, the inverter delay is 50 picoseconds and the exclusive-OR delay is approximately 120 picoseconds. Thus, the preferred slew rate is approximately 880 picoseconds. For signals transmitted above the rate of 600MHz, the signal slew rate is preferably less than 110% of the signal

cont B4

rate. The preferred slew rate for exponential signals is slightly faster if the signal reaches 75% of its final value earlier than ¾ of the transition time. The differential signals preferably cross half way through the voltage transition. At around ¾ of the way through the voltage transition, the signals have a difference of about 250mv which can be converted quickly to a large swing signal. To avoid noise amplification and to prevent signal coupling to the receiver output upon receipt non-transitioning single-ended signals, the transition time between 75% and the final signal value is preferably higher than the sum of two inverter delays and the exclusive-OR delay. It will be appreciated that the slew rate can go as fast as it takes amplified noise to reach the output of the comparator 410 whose output is coupled to the output terminal 420. That is, upon receiving a non-transitioning signal, the switches 415 switch state before the comparator output changes state based on noise amplification. The output of the currently coupled comparator 410 approaches an undetermined (noise amplified) state. The switches 415 must switch states before the undetermined output becomes available. It will be further appreciated that device mismatches, manufacturing tolerances and signal reflection will affect the speed at which the output of the comparator 410 reaches the undetermined state. As the technology improves, gate delays, faster slew rates and faster signal rates will be achievable.

The paragraph beginning at **page 22, line 12** has been amended to read as follows:

B5

FIGs. 8A and 8B are schematic diagrams illustrating circuit details corresponding to comparators 435 of FIG. 4. Each comparator 435 includes a differential amplifier 802 (FIG. 8A) or 852 (FIG. 8B) similar to the differential amplifier 702 of FIGs. 7A and multiple inverters 804 (FIG. 8A) or 854 (FIG. 8B) in series. The full rail output signals of the comparators 802 and 852 (VT1, VT2, VT3, /VT1, /VT2 & /VT3) are transmitted to all the single-ended receivers' XORs 425 (FIG. 4). Selection of VT1, VT2 or VT3 is determined based on testing for signal speed substantially equal to that of the receiver 405 output signal SN generation path.

The paragraph beginning at **page 22, line 20** has been amended to read as follows:

B6

FIG. 9 (9-1 and 9-2) is a schematic diagram illustrating receivers 405 with individually adjustable delays to eliminate skew during transmission and to convert small swing to large swing by comparators 410. To tune the operating frequency or voltage swing for optimum performance, each receiver 405 has a register 905 for storing data to enable delivery of one of the three VT1 & /VT1, VT2 & /VT2 or VT3 & /VT3 to the XOR 425 (FIG. 4).

The paragraph beginning at **page 23, line 15** has been amended to read as follows:

B7

By using devices with very low power dissipation and close physical packing, the bus can be made as short as possible, which in turn allows for short propagation times and high data rates. As shown in FIG. 2B, the resistor-terminated controlled-impedance transmission lines can operate at signal rates of 1Ghz (1ns per cycle). The characteristics of the transmission lines are strongly affected by the loading caused by integrated circuits like DRAMs mounted on the bus. These integrated circuits add lumped capacitance to the lines, which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the bus impedance is likely to be on the order of 25 ohms and the propagation velocity of 7.5cm/ns. Care should be taken not to drive the bus from two devices at the same time. So for buses less than about 12cm, one dead cycle (e.g., 2ns) is needed to settle the bus for switching from one driver to another driver. For longer buses, more than one cycle may be needed for the signals to settle down before a new transmitter can drive the signal. Unlike RAMBUS, the length of the bus does reduce operating frequency in burst mode from the same device.

<u>**In The Claims:**</u>

Please amend *EXISTING* claims **1, 6, 15** and **23** to read as follows:

B8 Sub C1

1. (Twice Amended) A method of detecting a transition in an incoming signal from a known previous logical state, comprising:

obtaining an oscillating reference;